What we claim is:

1. A differential current output unit, comprising:

a difference input circuit that includes

a first constant current source for providing a first constant current,

a first and a second differential amplification transistors for amplifying an inputted differential voltage so as to distribute said first constant current among said differential amplification transistors,

a first current mirror source transistor for generating a first voltage (referred to as first mirror source voltage) proportional to a first current flowing through said first differential amplification transistor, and

a second current mirror source transistor for generating a second voltage (referred to as second mirror source voltage) proportional to a second current flowing through said second differential amplification transistor;

a current subtraction circuit that includes

a first mirror transistor (referred to as first mirror target transistor) for flowing therethrough a first mirror current that is M times said first current I1 in response to said first mirror source voltage, with M being a first predetermined mirror ratio, and

a second mirror transistor (referred to as second mirror target transistor)for flowing therethrough a second mirror current that is M times said second current I2 in response to said second mirror source voltage, wherein said subtraction circuit is adapted to output a

difference current that is the difference between said first mirror current and second mirror current;

a delivery circuit for generating a current output instruction signals in accord with the magnitude of said difference current and for delivering said current output instruction signals in accord with the polarity of said difference current; and

a current output circuit having a multiplicity of output transistor circuits each including a third mirror source transistor that is enabled by one of said current output instruction signals and a third mirror target transistor for flowing therethrough an output current that is N times the current flowing through said third mirror source transistor, with N being a second predetermined mirror ratio, wherein said current output circuit is adapted to supply an output current to a load in a positive or a negative direction in accord with the polarity and the magnitude of said current instruction signals.

2. The differential current output unit according to claim 1, further comprising a current level setting circuit for controlling the current level of said first constant current source.

3. The differential current output unit according to claim 2, wherein

said delivery circuit includes

a first and a second delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has negative polarity, and

a third and a fourth delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has positive polarity;

said current output circuit includes

a first output transistor circuit for flowing therethrough an output current in response to a first current output instruction signal received from said first delivery transistor circuit,

a second output transistor circuit for flowing therethrough an output current in response to a second current output instruction signal received from said second delivery transistor circuit,

a third output transistor circuit for flowing therethrough an output current in response to a third current output instruction signal received from said third delivery transistor circuit, and

a fourth output transistor circuit for flowing therethrough an output current in response to a fourth current output instruction signal received from said fourth delivery transistor circuit; and

said current output circuit is adapted to establish

a first load current path for flowing the output current of said first output transistor circuit to an external load and flowing the output current of said second transistor circuit from said external load, and

a second load current path, opposite in direction with respect to said first load current path, for flowing the output current of

said third output transistor circuit to said external load and flowing the output current of said fourth output transistor circuit from said external load.

4. The differential current output unit according to claim 3, wherein each of said first through fourth output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit, and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, where N is said second predetermined mirror ratio.

5. The differential current output unit according to claim 3, wherein

each of said first and third output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor; and

each of said second and fourth output transistor circuits includes a mirror source transistor controlled by a respective current output instruction signal received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is $N \times \alpha$ times the current flowing through said mirror source transistor, wherein $N \times \alpha$ is a third mirror ratio with N being said second mirror ratio and α being an arbitrary number other than 1.

6. The differential current output unit according to claim 3, wherein

each of said first through fourth output transistor circuits includes a first current mirror circuit having a fourth predetermined mirror ratio Q and controlled by a respective current output instruction signal received from said delivery circuit, and a second current mirror circuit having a fifth predetermined mirror ratio P and controlled by the output current of said first current mirror circuit.

7. The differential current output unit according to claim 1, wherein

said current subtraction circuit has

said first mirror target transistor serially connected at a node to a second constant current source for supplying a second constant current so as to output a first difference current from said node in accord with said difference current, and

said second mirror target transistor serially connected at a node to a third constant current source for supplying the second constant current so as to output a second difference current of opposite polarity with respect to said first difference current from the node of these transistors.

8. The differential current output unit according to claim 7, further comprising a current level setting circuit for simultaneously controlling the current levels of said first, second, and third constant current sources by the same ratio.

9. The differential current output unit according to claim 8 wherein

said delivery circuit includes

a first and a second delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has negative polarity, and

a third and a fourth delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has positive polarity;

said current output circuit includes

a first output transistor circuit for flowing therethrough an output current in response to a first current output instruction signal received from said first delivery transistor circuit,

a second output transistor circuit for flowing therethrough an output current in response to a second current output instruction signal received from said second delivery transistor circuit,

a third output transistor circuit for flowing therethrough an output current in response to a third current output instruction signal received from said third delivery transistor circuit, and

a fourth output transistor circuit for flowing therethrough an output current in response to a fourth current output instruction signal received from said fourth delivery transistor circuit; and

said current output circuit is adapted to establish

a first load current path for flowing the output current of said first output transistor circuit to an external load and flowing the output current of said second transistor circuit from said external load, and

a second load current path, opposite in direction with respect to said first load current path, for flowing the output current of said third output transistor circuit to said external load and flowing the output current of said fourth output transistor circuit from said external load.

10. The differential current output unit according to claim 9, wherein each of said first through fourth output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, with N being said second predetermined mirror ratio.

11. The differential current output unit according to claim 9, wherein

each of said first and third output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, and

each of said second and fourth output transistor circuits includes a mirror source transistor controlled by a respective current

output instruction signal received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is N× α times the current flowing through said mirror source transistor, wherein N× α is a third mirror ratio with N being said second mirror ratio and α being an arbitrary number other than 1.

12. The differential current output unit according to claim 9, wherein

each of said first through fourth output transistor circuits includes a first current mirror circuit having a fourth predetermined mirror ratio Q and controlled by a respective current output instruction signal received from said delivery circuit, and a second current mirror circuit having a fifth predetermined mirror ratio P and controlled by the output current of said first current mirror circuit.

13. The difference current output unit according to claim 1, wherein said current subtraction circuit has

said first mirror target transistor connected in series at a node with a first subtraction transistor for flowing therethrough a current that is M times said second current in accord with said second mirror source voltage to thereby output from said node a first difference current in accord with said difference current, and

said second mirror target transistor connected in series at a node with a second subtraction transistor for flowing therethrough a current that is M times said first current in accord with said first mirror source voltage to thereby output from said node a second difference current having the same magnitude as, but the opposite

polarity to, said first difference current, wherein M is said second mirror ratio.

14. The differential current output unit according to claim 13, wherein

said delivery circuit includes

a first and a second delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has negative polarity, and

a third and a fourth delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has positive polarity;

said current output circuit includes

a first output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said first delivery transistor circuit,

a second output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said second delivery transistor circuit,

a third output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said third delivery transistor circuit, and

a fourth output transistor circuit for flowing therethrough an output current in response to a current output

instruction signal received from said fourth delivery transistor circuit; and

said current output circuit is adapted to establish

a first load current path for flowing the output current of said first output transistor circuit to an external load and flowing the output current of said second transistor circuit from said external load, and

a second load current path, opposite in direction with respect to said first load current path, for flowing the output current of said third output transistor circuit to said external load and flowing the output current of said fourth output transistor circuit from said external load.

15. The differential current output unit according to claim 14, wherein each of said first through fourth output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit, and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, where N is a second predetermined mirror ratio.

16. The differential current output unit according to claim 14, wherein

each of said first and third output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit and a mirror

target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, and

each of said second and fourth output transistor circuits includes a mirror source transistor controlled by a respective current output instruction signal received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is $N \times \alpha$ times the current flowing through said mirror source transistor, wherein $N \times \alpha$ is a third mirror ratio with N being said second mirror ratio and α being an arbitrary number other than 1.

17. The differential current output unit according to claim 14, wherein

each of said first through fourth output transistor circuits includes a first current mirror circuit having a fourth predetermined mirror ratio Q and controlled by a respective current output instruction signal received from said delivery circuit, and a second current mirror circuit having a fifth predetermined mirror ratio P and controlled by the output current of said first current mirror circuit.

18. The differential current output unit according to claim 1, wherein

said delivery circuit includes

a first and a second delivery transistor circuits for respectively outputting a current output instruction signal that is controlled in accordance with said difference current when said difference current has negative polarity, and

a third and a fourth delivery transistor circuits for respectively outputting a current output instruction signal that is

controlled in accordance with said difference current when said difference current has positive polarity;

said current output circuit includes

a first output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said first delivery transistor circuit,

a second output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said second delivery transistor circuit,

a third output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said third delivery transistor circuit, and

a fourth output transistor circuit for flowing therethrough an output current in response to a current output instruction signal received from said fourth delivery transistor circuit; and

said current output circuit is adapted to establish

a first load current path for flowing the output current of said first output transistor circuit to an external load and flowing the output current of said second transistor circuit from said external load, and

a second load current path, opposite in direction with respect to said first load current path, for flowing the output current of said third output transistor circuit to said external load and flowing

the output current of said fourth output transistor circuit from said external load.

19. The differential current output unit according to claim 18, wherein each of said first through fourth output transistor circuits includes a mirror source transistor controlled by respective current output instruction signals received from said delivery circuit, and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor, where N is a second predetermined mirror ratio.

20. The differential current output unit according to claim 18, wherein

each of said first and third output transistor circuits includes a mirror source transistor controlled by a respective current output instruction signal received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is N times the current flowing through said mirror source transistor; and

each of said second and fourth output transistor circuits includes a mirror source transistor controlled by a respective current output instruction signal received from said delivery circuit and a mirror target transistor for flowing therethrough a current that is $N \times \alpha$ times the current flowing through said mirror source transistor, wherein $N \times \alpha$ is a third mirror ratio with N being said second mirror ratio and α being an arbitrary number other than 1.

21. The differential current output unit according to claim 18, wherein

each of said first through fourth output transistor circuits includes a first current mirror circuit having a fourth predetermined mirror ratio Q and controlled by respective current output instruction signals received from said delivery circuit, and a second current mirror circuit having a fifth predetermined mirror ratio P and controlled by the output current of said first current mirror circuit.